7.3 Signal-Margin-Screening for Multi-Mb MRAM

H. Hönigschmid[1], P. Beer[1], A. Bette[1], R. Dittrich[1], F. Gardic[2], D. Gogl[1], S. Lammers[1],J. Schmid[1], L. Altimime[1], S. Bournat[2], G. Müller[1]

[1]Infineon, Munich, Germany
[2]Altis Semiconductor, Corbeil Essonnes, France

Magnetoresistive RAM (MRAM) technology combines advantages of established Flash, SRAM and DRAM memory platforms such as fast read/write performance [1], non-volatility, and high write endurance [2].

As MRAM technology is maturing [3, 4] there is a need for developing a strategy to identify and replace marginal bits during read/write operation in order to have stable chip operation. In this paper, the methodology for read/write signal margin screening and corresponding circuit techniques used in a 0.18µm 16Mb MRAM chip are described.

In order to achieve high read signal margins a perfectly symmetric sensing scheme using an improved capacitive balancing concept is implemented. The sensing scheme of the 16Mb MRAM chip is shown in Fig. 7.3.1. The column select circuits (CSL) connect the data BLs and the reference BLs of the memory array to the data inputs (In0, In1) and reference inputs (RefIn0, RefIn1) of the sense amplifier. The BLs are clamped to the optimum read voltage by source follower devices N0 - N3. The resulting cell currents correspond to the states of the data and reference cells within the memory array (I_{data}, I_{ref}) and are translated into a differential voltage at the current mirror load devices P0/P1 and P2/P3. The MRAM cells connected to the reference BLs are programmed to opposite states (R_L, R_H) and shorted together at the RefIn and RefLoad nodes. This ensures that the current through each transistor diode of the current-mirror load devices (P1, P2) is an ideal mid-point reference $I_{ref} = (I_{ref0} + I_{ref1}) / 2$. The differential voltage at the current-mirror load devices P0/P1 and P2/P3 is converted into a digital output signal by comparators Comp0 and Comp1 (only details of Comp0 shown for clarity).

The sensing circuit is a fully balanced symmetric design from the CSL up to the current-mirror load devices of the sense amplifier. The capacitive imbalance of the Load and RefLoad nodes of the current-mirror devices P0/P1 and P2/P3 is compensated by the comparator input transistors P4/P5. In order to achieve the same capacitive load at nodes Load0 and RefLoad, the device width of transistor P5 has to be $3*W_P$ assuming a device width of W_P for transistors P0, P1, and P4. In addition, the drain/source voltage sensitivity of the gate capacitance of P5 requires the drain potential V_{bal} to be approximately the potential of RefLoad during sensing. This is reliably achieved by sizing of transitor N5, which is 3 times the width of N4.

In order to address the potential loss of marginal bits in the 16Mb chip caused by device mismatches of the sensing circuit an offset calibration scheme is implemented in the comparators of the sense amplifiers. As illustrated in Fig. 7.3.2 (for comparator Comp0 of Fig. 7.3.1), the width of current-mirror devices N4 and N5 can be increased by additional calibration transistors shown in SACAL. A closed switch CAL0 adds transistor width to N5. The addition of more or less transistor width to N4 using switches CAL1 – CAL7 allows for correction of positive or negative offsets. Calibration transistors are deselected for closed switches bCAL and open switches CAL.

As explained in Fig. 7.3.3, after compensation of the SA offset, the weak read bits can be identified by applying suitable read voltages V_{READ} at the MRAM cell R_{MTJ}. A source-follower-type BL clamp device supplies a constant voltage $V_{READ} = V_{BLC} – V_{GS}$ to the BL, whereas the BL clamp voltage V_{BLC} can be controlled at the generator via test mode. Lower V_{BLC} voltages lead to a lower signal current due to a lower voltage applied at the MRAM cell whereas higher V_{BLC} voltages lead to a higher voltage at the MRAM cell. However due to the decreasing magneto resistance (MR) at increasing voltages, a lower signal current is generated as well. Through this method identified failing (weak) bits of the 2 operating conditions (V_{BLC}=0.56V, V_{BLC}=0.89V) above/below the default V_{BLC} value (V_{BLC}=0.76V) are superposed and replaced with redundant bits, leading to a significantly increased read signal margin of ≈300mV.

Figure 7.3.4 illustrates the implemented local write current trimming architecture. A 128kb array-specific write-current-tuning scheme is used to compensate for imbalances and variations in the write path caused by cell/wiring parameter variations and current-mirror mismatches.

Two global current sources (for I_{BL} and I_{WL}) are located in the centre of the left peripheral circuit block of the 16Mb. The global current sources receive a constant reference current I_{ref} from a bandgap circuit (6µA) and generate the global write reference currents I_{global} that will be trimmed ($I_{trimmed}$) and distributed to the local WL and BL write current sources of the 128kb arrays. To minimize active power and area needed for wiring, 3 local write current trimming circuits (1 for I_{WL}, 2 for the data-dependent I_{BL}) are located at the left of each row of 128kb arrays providing individually adjusted write currents for the 16 arrays located in 1 row. As it is further explained in Fig. 7.3.4, $I_{trimmed}$ can be adjusted in 30 individual steps of ≈1.6% of I_{global} using control signals INCR/DECR and the tuning information stored in the fusebank, resulting in $0.77\times I_{global} \le I_{trimmed} \le 1.23\times I_{global}$.

Figure 7.3.5 displays the measurement results of the proposed local-array-tuning concept. Without local array tuning a write margin of ≈7Oe in terms of external field is achieved whereas some array blocks already showed a marginal/failing signature. The write margin of the 16Mb MRAM chip could be significantly improved to ≈17Oe using the proposed local array trimming architecture.

A summary of the main features of the chip is shown in Fig. 7.3.6. The proposed methodology provides fully functional chips at V_{ext}=3.3V using a wafer-level screen test including half select disturb pattern. Figure 7.3.7 shows a die micrograph of the 16Mb MRAM chip.

Acknowledgement:
The circuit concepts described in this paper were developed and implemented within the IBM-Infineon MRAM Development Alliance.

References:
[1] A. Bette et al., "A High-Speed 128kbit MRAM Core for Future Universal Memory Applications," *Dig. Symp. on VLSI Circuits,* pp. 217-220, June, 2003.
[2] S. Tehrani et al, "Magnetoresistive Random Access Memory Using Magnetic Tunnel Junctions," *IEEE Proceedings*, vol. 91, pp. 703-714, May, 2003.
[3] D. Gogl et al, "A 16Mb MRAM Featuring Bootstrapped Write Drivers," *IEEE J. Solid-State Circuits,* vol. 40, pp. 902-908, Apr., 2005.
[4] T. Andre et al, "A 4Mb 0.18µm 1T1MTJ Toggle MRAM Memory," *ISSCC Dig. of Tech. Papers,* pp. 44-45, Feb., 2004.

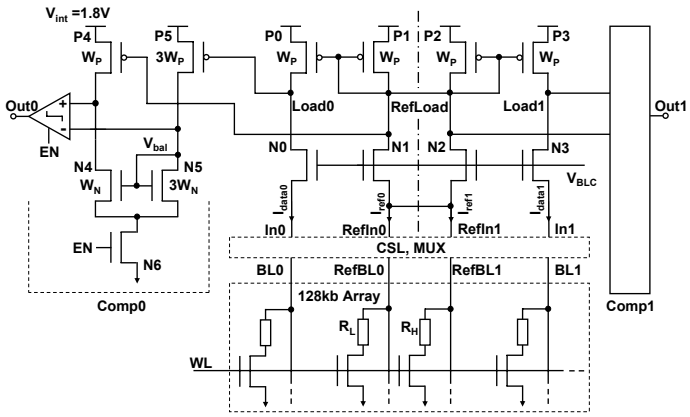


Figure 7.3.1: Sensing circuit.

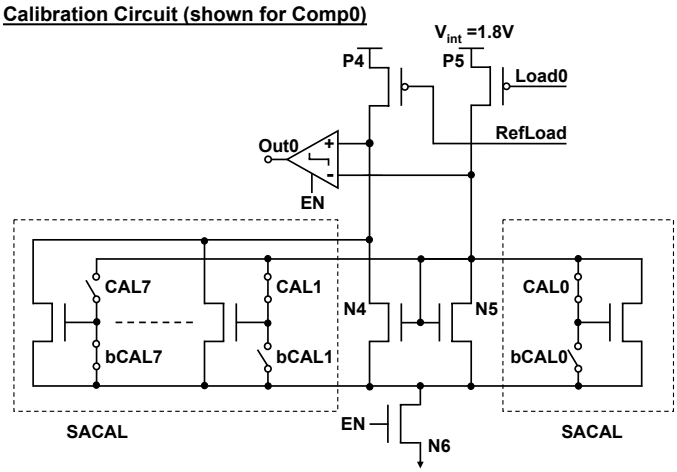


Figure 7.3.2: SA offset calibration.

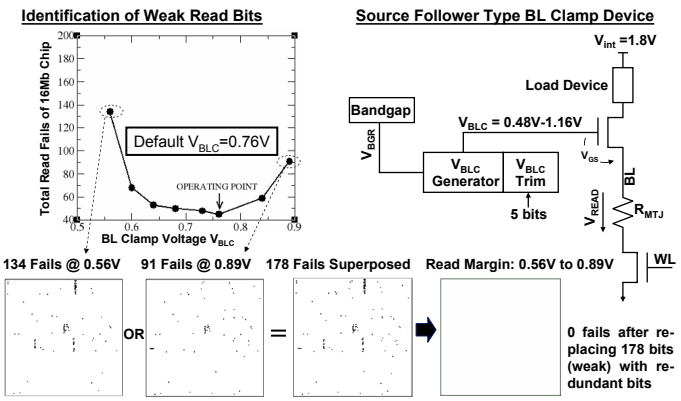


Figure 7.3.3: Signal margin screening for read.

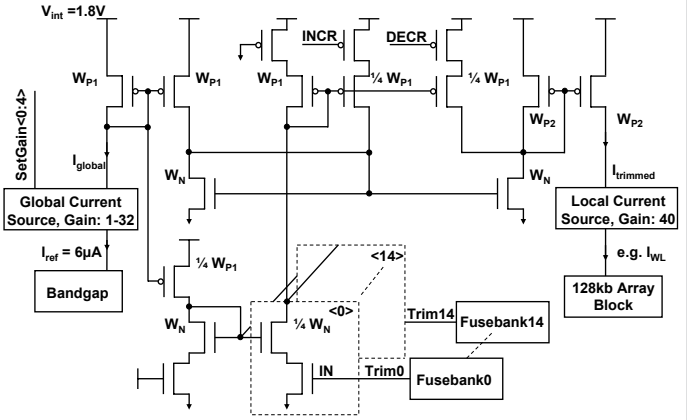


Figure 7.3.4: Local Write Current Trimming.

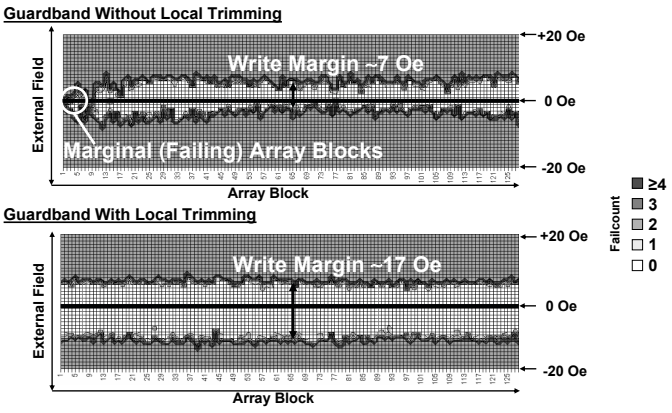
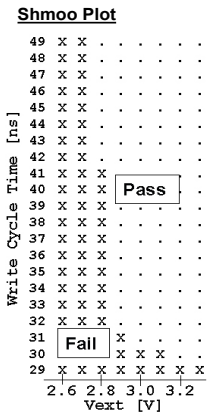


Figure 7.3.5 : Results of Local Write Current Trimming.



Main Features

Base Technology	3-Cu, 0.18µm CMOS
Process Adder	3 MRAM-specific levels
Cell / Chip Size	1.42µm² / 79mm²
Ext. Supply Voltage V_{ext}	3.3V
Interface	x16 asynch. SRAM
Package	48pin BGA (SRAM comp.)

Figure 7.3.6: Chip Performance and Main Features.

Continued on Page 644

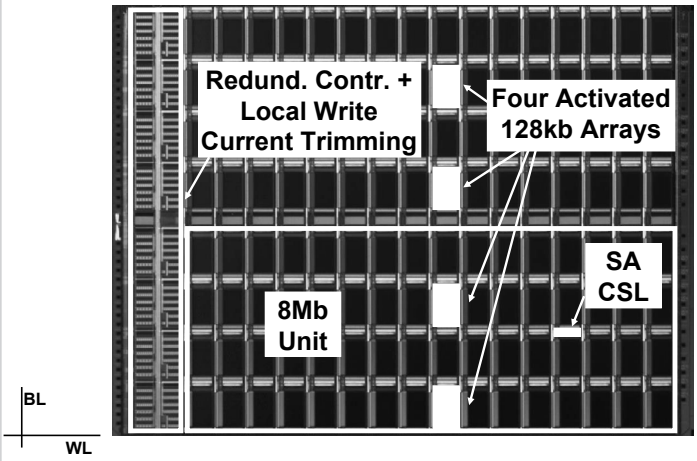


Figure 7.3.7: 16Mb MRAM die micrograph.

